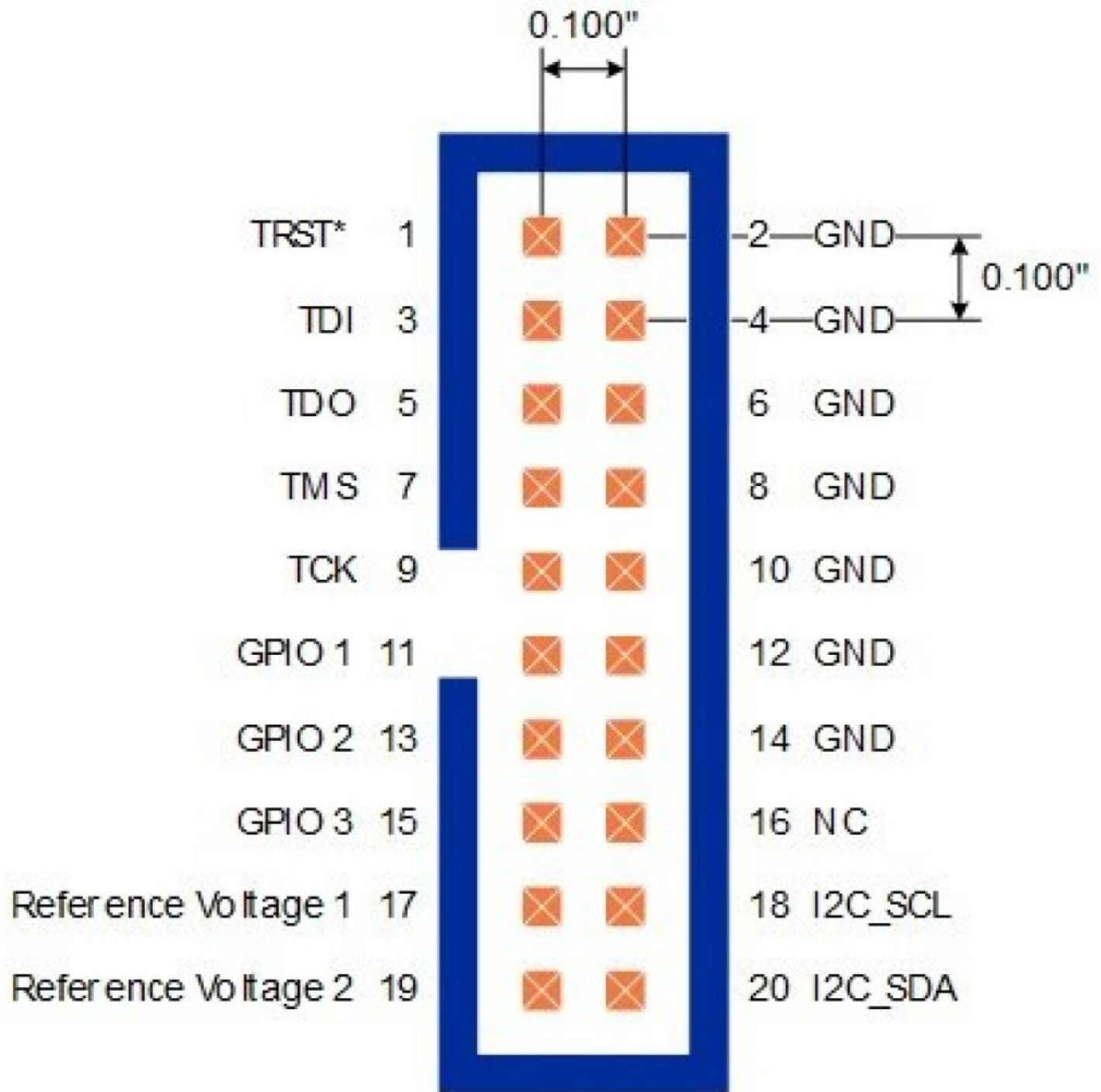


JTAG TAP Controller Connectors Corelis, Inc



Cerritos, California May 10, 2022 (Issuewire.com) - This primer provides a brief overview of JTAG devices—basic chip architecture, essential capabilities, and common system configurations.

JTAG Chip Architecture

The IEEE-1149.1 [JTAG](http://Issuewire.com) standard defines how IC scan logic must behave to achieve interoperability among components, systems, and test tools. ICs consist of logic cells, or boundary-scan cells, between

the system logic and the signal pins or balls that connect the IC to the PCB. Each cell provides specific test capabilities—some cells can be used as input, others as output, and some are bidirectional.

The boundary-scan cells within a device are connected together to form a shift register, which is accessed through a serial test data input (TDI) and test data output (TDO) interface. The Test Access Port (TAP), consisting of 4 required signals and an optional reset signal, is the primary interface to the test controller which provides access to the logic.

JTAG Instructions

IEEE-1149.1 specifies mandatory instructions—to be fully [JTAG](#) compliant, devices must utilize these instructions.

EXTEST

The EXTEST instruction is used to perform interconnect testing. When the EXTEST instruction is used, the mandatory boundary-scan register is connected between TDI and TDO, and the device is placed in an “external” test mode. In this mode, boundary-scan output cells will drive test data onto the device pins and input cells will capture data from device pins—this is the main instruction used for boundary-scan testing.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is similar to EXTEST but allows the boundary-scan device to remain in mission/functional mode while still connecting the boundary-scan register to TDI and TDO. When the SAMPLE/PRELOAD instruction is used, the boundary-scan register is accessible through data scans while the device remains functional. This is also useful for preloading data into the boundary-scan register without interrupting the device’s functional behavior, prior to executing the EXTEST instruction.

BYPASS

When the BYPASS instruction is used, TDI and TDO are connected to a single-bit register that bypasses the longer boundary-scan register of the device—hence the name. BYPASS is very useful for reducing the overall length of a boundary-scan chain by eliminating devices that do not need to be involved in the current action. Devices that are given the BYPASS instruction remain in mission/functional mode while allowing serial data to flow through to the next device in the chain.

JTAG TAP Controller

The TAP controller as defined by the IEEE-1149.1 standard uses a 16-state finite state machine controlled by a test clock (TCK) and test mode select (TMS) signals. Transitions are determined by the state of TMS on the rising edge of TCK.

Two analogous paths through the state machine are used to capture and/or update data by scanning through the instruction register (IR) or through a data register (DR).

JTAG Interface

The physical JTAG interface, or test access port (TAP) consists of four mandatory signals and one

optional asynchronous reset signal. Table 1 below summarizes the JTAG TAP signals.

Many TAP interfaces will employ signals in addition to those required by the JTAG standard. For example, on-chip debugging applications may include signals for an asynchronous halt and reset, while in-system-programming applications may increase programming speed by taking advantage of additional pins for time-critical functions such as toggling the write enable signal or polling a ready/busy signal.

Here's the video for understanding easily -

<https://youtu.be/uQs32JjZrhs>

JTAG Connectors

There is no single standard JTAG interface connector or JTAG pinout—physical characteristics such as pin spacing, interface voltage, and pin order vary among devices. Some TAP implementations may include additional signals such as a reference voltage, general-purpose input/output (GPIO), or even serial bus signals.

BSDL Files

Boundary-Scan Description Language (BSDL) files are used to describe the boundary-scan behavior and capabilities of a given device. Originally designed as a subset of VHDL, the BSDL format has been extended to add additional features and is not strictly VHDL compliant. The BSDL describes important properties of a given device's boundary-scan functions, including:

Which JTAG standards are supported by the device.

Signal mapping and package information.

Available instructions, and which registers those instructions access.

The type of boundary-scan cell is available for each signal.

Information about signals that affect compliance with the standard.

Design warnings and notes.

Over time, the BSDL format has also been extended to include additional information; BSDL files may include descriptions of AC (IEEE-1149.6) testing capabilities, sequences in procedural description language (PDL) format, and information about an electronic chip identifier (ECID), and more. BSDLs include statements that specify which standards are supported to allow automated tools to utilize supported features.

JTAG Scan Chain

JTAG devices may be daisy-chained within a system and controlled simultaneously. Boundary-scan test software can utilize one component to drive signals that will be sensed on a second component, verifying continuity from pin to pin. Devices can be placed in BYPASS mode to shorten the overall length of the chain to reduce test time. More complex designs may utilize additional circuitry or a

dedicated JTAG bridge to selectively configure a scan chain that contains multiple devices, or even multiple sub-assemblies.

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