

MOSCHIP ANNOUNCES MULTI-PROTOCOL LONG RANGE 8G SERDES PHY in 28nm

Supporting PCIe Gen3.1, XAUI, CEI, SATA3, KX4, Display Port, MIPI M-PHY Standards

NEW RELEASE

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California, Santa Clara, Oct 12, 2021 ([Issuewire.com](https://www.issuewire.com)) - MosChip Technologies Limited, a semiconductor and system design services company, unveils today a multi-protocol Long Range (LR) 8G SerDes PHY in 28nm. MosChip has over a twenty-year track record in designing semiconductor IP, products, and SoCs for IoT, networking, industrial, and consumer applications.

[MosChip](#) was the first fabless semiconductor company out of India and has developed many connectivity-based products that were fabricated at leading foundries and shipped in millions of units. With the acquisition of Gigacom in 2018, the company has developed niche expertise in the areas of analog, mixed-signal design, high-speed serial interfaces, and IP portfolio which includes silicon proven SerDes, PLLs, and Data converters. The multi-lane multi-protocol LR 8G PHY IP is part of MosChips' high-performance multi-rate transceiver portfolio, meeting the growing needs for small footprint, low-power consumption, and low latency edge applications.

“Our LR 8G PHY is implemented as a self-contained protocol-agnostic Physical Medium Attachment (PMA) IP with a flexible digital I/F on the system side that could be made compatible with most PCS standard definitions that exist in the industry today,” said [Albert Vareljian](#), Chief Architect at MosChip. “PHY is based on our innovative self-tuning architecture and fully adaptive continuous-time equalizer with automatic gain control analog front end (AFE) combined with adaptive multi-tap decision feedback equalization (DFE) to cover channel variations and PVT range”.

PHY is fully configurable for programmable lane enable/disable and choices of macros pre-configured for 1 to 16 lanes and supports various debug features such as serial and parallel loopback. The 8G PHY

macro is backward compatible and can operate in compliance with PCI Gen1/2, SATA 1/2 specifications. It includes a PCIe standard multi-lane interface. No external passive components are required, saving area at the system level and pin count at the chip level.

“This is a major milestone for MosChip, which highlights our strategic focus to develop niche SerDes PHY IP that is customizable as per customer end applications,” said [Venkata Simhadri](#), MD/CEO of MosChip. With the addition of silicon-proven LR 8G PHY to our portfolio, we are well positioned to provide both custom/porting PHY IP services and turn-key mixed-signal ASIC solutions.

LR 8G PHY macro deliverables include a complete set of logical views, physical views, documentation, Verilog model, a UVM-based verification environment, an abstract view, liberty files, netlist, GDSII, and flip-chip bump/ball map plans.

About MosChip

MosChip Technologies Limited is a publicly traded semiconductor and system design services company headquartered in Hyderabad, India, with 700+ engineers located in silicon valley-USA, Hyderabad, and Bangalore. MosChip provides turn-key digital and mixed-signal ASICs, design services, SerDes IP, and embedded system design solutions. Over the past 2 decades, MosChip has developed and shipped millions of connectivity ICs. For more information, visit moschip.com

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